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| **Final Project Report** | |
| Student ID: 123456789、987654321 | Name: 王大明、王小明 |

1. Design concept (You may write the report in Chinese):

* Please provide block diagrams of the overall hardware architecture and each component. Please explain the purpose and the way they work together.
* Please provide state diagram of your FSM (if any), and its detailed description. If no FSM is used in your design, please explain your control flow.
* Please explain your dataflow in detail.

(How many cycle do you need to read/write weights/activations? How do you compute the result in how many cycle? What data do you keep in register for later reuse? … please do NOT simply answer these questions in short. Instead, provide a complete explanation of your design.)

* Please explain the usage of the free-to-use space in the SRAMs.
* Any additional information you want to provide.

1. Result

|  |  |  |
| --- | --- | --- |
| Item | Description | Unit |
| RTL simulation | PASS | --- |
| Gate-level simulation | FAIL | --- |
| Gate-level simulation clock period | 10 | ns |
| Gate-level simulation latency | 10000 | cycles |
| Total cell area | 80000 |  |

1. Contribution (skip this part if you are in a 1-person group)

|  |  |  |
| --- | --- | --- |
| Item | Student1 | Student2 |
| Architectural design | 50% | 50% |
| Coding | 40% | 60% |
| Report writing | 60% | 40% |
| … (you are free to adjust or add the items base on your situation) | … | … |

1. END\_CYCLE (optional)

* If you need a larger END\_CYCLE than the default, please let us know what value you are using.

|  |  |
| --- | --- |
| END\_CYCLE |  |

1. Others (optional)
   * Suggestions or comments about this class to teacher or TA.